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RESEARCH ARTICLE

A Pencil Shaped 9-Level Multilevel Inverter With Voltage Boosting Ability: Configuration and Experimental Investigation

SHEIKH T. MERAJ¹, M. S. ABD RAHMAN²,

NOR ZAIHAR YAHAYA¹⁰, (Senior Member, IEEE), PIN JERN KER¹⁰, (Senior Member, IEEE), TOUHID M. HOSSAIN¹⁰³, M. S. HOSSAIN LIPU¹⁰⁴, KASHEM M. MUTTAQI¹⁰⁵, (Senior Member, IEEE), AND

M. A. HANNAN[®]², (Senior Member, IEEE)

¹Department of Electrical and Electronic Engineering, Universiti Teknologi PETRONAS, Seri Iskandar, Perak 32610, Malaysia

²Department of Electrical Power Engineering, College of Engineering, Universiti Tenaga Nasional, Kajang, Selangor 4300, Malaysia

³Department of Computer and Information Sciences, Universiti Teknologi PETRONAS, Seri Iskandar, Perak 32610, Malaysia

⁴Department of Electrical and Electronic Engineering, Green University of Bangladesh, Dhaka 1207, Bangladesh ⁵School of Electrical, Computer and Telecommunication Engineering, University of Wollongong, Wollongong, NSW 2522, Australia

 $Corresponding \ authors: M. \ A. \ Hannan \ (hannan@uniten.edu.my) \ and \ Nor \ Zaihar \ Yahaya \ (norzaihar_yahaya@utp.edu.my) \ A. \ Hannan \ (hannan@uniten.edu.my) \ and \ Nor \ Zaihar \ Yahaya \ (norzaihar_yahaya@utp.edu.my) \ A. \ Hannan \ (hannan@uniten.edu.my) \ A. \ (hannan \ (hannan@uniten.edu.my) \ (hannan \ (hannan\ (hannan \ (hannan\ (hannan \ (hannan \ ($

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ABSTRACT A comprehensive study of a minimized component pencil shaped (PS) 9-level inverter constructed with just two DC supplies is presented in this research. Many of the suggested low component multilevel inverters (MLIs) use DC supplies that are not being used appropriately along with additional conducting switches. Since this proposed MLI has a reduced quantity of power electronic switches, it is more efficient. The architecture may be expanded to a modular higher voltage level inverter, which uses less DC supplies and uses them correctly without the need of an extra H-bridge circuit. To determine their optimum capabilities, the proposed inverter parameters' simplified formulas are constructed. Furthermore, the extended model of the proposed architecture is used to generate an optimum PSMLI design for lowering the total standing voltage (TSV) of the inverter. To demonstrate its advantages over recent MLIs of similar types, comparison studies are given to justify the proposed inverter. Through proper simulation and laboratory experiment, the MLI obtained a higher efficiency of 95.54%. On the other hand, the optimized 17-level version of PSMLI obtained total harmonic distortions (THD) of only 5.15% which successfully attained IEEE 519 standard performance.

INDEX TERMS Multilevel inverter, power electronics, switched capacitor, voltage boost, nearest level control.

I. INTRODUCTION

Multilevel inverters offer a consistent and precise output voltage. In the realm of power electronics, researchers find MLIs that have different shapes to be very interesting. Recently, a large diversity of configurations has developed in power systems, with variety of applications. In medium and high-power systems, including power grid, electrical vehicles [1], drive systems [2], active power filters [3], [4],

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wind turbines [5], solar systems [6], and HVDC for transmission lines [7], MLIs are the preferred inverter above standard two-level inverters. Since MLIs generate multilayer voltage, they feature minimal harmonic profile and ripplefree output voltage. The cascade connection capabilities of MLIs confirms that the switches have minimal stress and electromagnetic interference, resulting in high efficacy for the system.

Multilevel inverters come in a variety of modules, for instance, Neutral Point Clamped (NPC), Flying Capacitor (FC), and Cascade H-bridge (CHB). Large capacitor voltage dips are observed in FC and NPC, resulting in imbalanced DC links and high voltage stress on the switches. CHB topologies, on the other hand, are suggested by researchers as a way to design configurations with fewer components. The fundamental disadvantage of typical CHB-MLIs is that they need a large number of separate DC sources and conductor switches to generate multilevel voltage. According to [8], MLIs can be divided into three different types depending on the structure and the magnitude of the DC supplies: which are asymmetrical, symmetrical, and hybrid MLIs. In the unipolar MLI topologies proposed in [9]-[12], H-bridge circuits with polarity generating capacity are necessary to acquire negative and positive voltage levels at the output provided by the level generating (LG) section. Although the LG section generated voltage become approximately double by the H-bridge, the power electronic switches of the H-bridge need to endure the highest voltage stress equivalent to the total DC-link voltage [13]. Switched-battery boost (SBB) MLI as reported in [14] reduces the switch count by using two DC supplies with one diode and a switch to generate just two voltage levels. However, to generate higher voltages, this MLI needs a greater number of DC supplies, and the levels can only be attained by combining the multiple sources. As an alternative, crisscross switched based inverters are proposed to generate greater voltage with fewer components The MLI using crisscross switched configuration as shown in [15] included the semi-half-bridge cell that employed a moderate number of DC sources and semiconductor switches to achieve a certain voltage level. Although these MLIs employ minimal DC sources, an extra H-bridge circuit is utilized that has high voltage stress and therefore, raised their total standing voltage (TSV).

Bipolar configurations are more appealing because of their intrinsic ability to create negative voltage stages without H-bridge circuit, which helps to reduce high TSV. A square shaped MLI module was proposed in [16] utilizing 4 DC sources and 12 switches to produce 17 voltage levels. Even though the MLI's structure has been established utilizing low rated switches, it uses asymmetrical DC sources. Thus, the TSV of this MLI is very high. Because of using 4 DC sources, it will require 4 transformers to provide galvanic isolation, that may increase the overall cost of the system significantly. Moreover, because of using asymmetric DC sources, it needs precise voltage balancing to maintain the constant voltage ratio among the DC sources which can induce control complexity. In comparison, the proposed MLI only used 2 symmetric DC sources and 10 switches to produce 9-level voltage. Thus, it has overcome all the issues associated with the MLI of [16]. A similar envelope type (E-type) topology can be observed in [17] where 10 switches and again 4 asymmetrical DC sources are used to generate 13-level. This topology has similar issues like the MLI in [16]. The configuration is redesigned by putting two capacitors in place of two DC supplies in the kite shaped MLI [18]. This MLI can produce 13-level voltage utilizing 2 more switches than the proposed MLI. However, it again utilized asymmetrical DC sources which has increased its TSV and induced voltage balancing issues. In [19], an inverter with 5 symmetric DC supplies and bidirectional switches is presented that couples two generic T-type inverter sub-modules with 4 cross connected switches and 4 DC supplies. Although this configuration solved the issue of asymmetrical DC sources of previous configurations, it still requires higher number of DC supplies. Additionally, this device has comparatively high TSV than the proposed MLI because of using the cross connected switches which bear the entire voltage stress of each T-type sub module. Ref [20], [21] present another two symmetrical configuration that makes extensive use of DC sources while prohibiting the use of asymmetric DC supplies. However, the cost of these devices is elevated because of using high number of isolated DC sources.

By implementing switched capacitors instead of DC sources, a new group of MLIs known as switched capacitor MLI (SCMLI) aims to reduce the number of components while also lowering the switching stress. This particular MLI group uses a blend of DC supplies and capacitors to produce sinusoidal voltage. Furthermore, higher voltage steps or voltage boosting can be obtained using the same DC sources. According to [22]–[27], SCMLI designs aim to substitute several DC supplies with capacitors. However, the increased number of switching devices are required in these MLIs to maintain capacitor voltages complicating the circuit configuration.

The study presented a novel MLI module using a clever combination of DC source, capacitors and switches. With the goal of achieving maximum voltage steps, switching devices and DC sources are implemented with enhanced power quality and cost-effectiveness in mind. Using only 2 switched capacitors and 2 DC supplies, this module can generate 9 levels output. To synthesize negative output levels, the suggested module doesn't need any extra circuit. As a result, the TSV of the MLI is greatly reduced.

The principal contributions of the manuscript can be stated as follows:

- 1. The proposed PSMLI module use reduced number of power electronic components compare to other MLIs available in the recent literatures.
- 2. Using its intelligent switching arrangement and current paths, it can generate negative voltage inherently without requiring any additional power components. Thus, TSV of the PSMLI has significantly decreased.
- 3. The proposed MLI requires fewer switching transitions to generate multilevel voltage because of utilizing a smart combination of switches, switched capacitors and DC-links.
- 4. The proposed MLI does not require any additional power components to balance the capacitor voltages. Thus, it has further optimized and simplified the structure making it cost effective.

The entire structure of manuscript is organized by dividing it into seven major sections. Section 2 discusses the state of



FIGURE 1. Schematic diagram of the proposed MLI.

the art, features, modularity, TSV, efficiency and power losses of PSMLI. The third section demonstrates the optimized structure of PSMLI and its advantages. Following that the next section presents a comprehensive comparative analysis with other MLIs. Section 5 presents results and discussions which includes simulation and experimental results. Finally, section 6 discusses the conclusions of the manuscript.

II. PSMLI AND ITS CONFIGURATION

The proposed module is built using a proper configuration of power electronic components to achieve maximum number of voltage levels using the DC sources and switched capacitors.

This topology uses the basic operation of switched capacitors to further increase and boost the voltage levels. Another challenge in this type of MLI would be to maintain the voltage of the capacitors without needing any additional circuit.

A. CONFIGURATION AND WORKING PRINCIPLE OF PSMLI The pencil shaped MLI (PSMLI) is build following the edifice of a pencil as depicted in Fig. 1. It has 3 principal segments which are represented using 3 color schemes. The first part is called the head (brown color), the 2nd segment is referred as the body (yellow color) and eraser is the final part (pink color).

The first section includes 2 unidirectional switches (S_1, S_2) . These serve as directional switches and the module's current path is determined by them. PSMLI, for example, will only produce positive voltage levels, if S_1 is switched on. However, when S_2 is turned on, it can typically generate negative voltage levels. The body part consists of 4 unidirectional switches (S_3, S_4, S_6, S_7) and 1 bidirectional switch (S_5), 2 DC source (V_{DC1} , V_{DC2}) and 2 switched capacitors (V_{C1} , V_{C2}). The switches S_3 and S_7 is utilized to avoid the short-circuit of capacitor V_{C1} and V_{C2} . The body part performs as the channel between the head and the eraser. The reverse current is blocked by the bidirectional switch S₅. The bottom part of PSMLI is an eraser shaped part that consists of 2 unidirectional switches (S_8, S_{10}) and 1 bidirectional switch (S_9) . It structurally looks like a T-type inverter and thus can generate negative levels without needing additional H-bridge unit. The MLI can produce



FIGURE 2. PSMLI's current path to produce 9-level voltage.



FIGURE 3. Operation of PSMLI using NLC technique.

9 levels voltage (\pm 4 levels, and 0 level) using the DC-links. PSMLI's power switches are cleverly implemented so that the capacitors and DC supplies are coupled through different current channels, requiring no additional circuit to balance out the voltage of the capacitors.

Table 1 shows the switching pattern while Fig. 2 illustrates the current routes of PSMLI. In addition, Fig. 3 shows the



FIGURE 4. TSV of PSMLI's each switch at various voltage levels.

TABLE 1. PSMLI's switching pattern.

	Output	Pattern of switching									
	V_{AB}	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}
els	4E	1	0	1	0	0	1	1	1	0	0
eve	3E	1	0	1	0	0	1	1	0	1	0
Ŧ	2E	1	0	0	0	1	0	0	1	0	0
	E	1	0	0	0	1	0	0	0	1	0
$+V_{C2}$	0(i)	1	1	0	0	1	1	1	0	0	0
$+V_{C1}$	0(ii)	0	0	1	0	1	1	0	1	0	1
~	- <i>E</i>	0	1	1	0	1	0	0	0	1	0
vels	-2E	0	1	1	1	0	0	0	1	0	0
Le	- 3E	0	1	1	1	0	0	0	0	1	0
I	- 4 <i>E</i>	0	1	1	1	0	0	1	0	0	1
Number on in eac	of turn h cycle	1	3	2	1	2	3	4	7	8	3

behave of the power switching components of the proposed PSMLI using the nearest level control (NLC) technique. It can be observed that zero voltage level is used to charge the DC capacitors. Table 1 also shows the number of times each switch turns on during one complete cycle of operation. The switching sequences of Table 1 confirm that switches $(S_1, S_2, S_3, S_4, S_5, S_6, S_{10})$ are turning with low frequency which has significantly reduced the TSV of the PSMLI. For each voltage level of PSMLI, a graphical depiction of the TSV of each switch for every voltage level is presented in Fig. 4. Thus, the TSV of the PSMLI is calculated to be 16 V_{DC}.

B. BMODULARITY OF SYMMETRIC MODULE

The proposed PSMLI's flexibility is verified in this section by showcasing its ability to generate higher number of voltage levels. This is done by extending the structure of the 9-level PSMLI inverter which is depicted in Fig. 5. Here, the ratio between the DC sources and the capacitors is unity. The extended structure is developed by extending the body part of PSMLI and which is then connected with another similar structure using cascaded connection as depicted in Fig. 5. The polarity is converted using 2 conduit switches which are placed between the main body and extended body of the PSMLI. These 2 switches will also function as the polarity



FIGURE 5. Modular PSMLI unit with x^{th} and z^{th} modules.

converter similar to the directional switches used in the head section of the PSMLI. The cascaded connection is established with z^{th} module to double the voltage producing ability. The x^{th} sub-modules incorporate 6 unidirectional switches, 1 bidirectional switch, 2 switched capacitors, and 2 DC sources. For a specific number of x^{th} module and z^{th} module, the number of voltage sources (N_{DC}), number of capacitors (N_C), number of power switches (N_P), and the voltage levels (N_V), TSV (N_{TSV}) can be determined as:

$$N_{DC} = N_C = 2(z + x + 1) \tag{1}$$

$$N_P = 4(3z + 2x + 3) \tag{2}$$

$$N_V = 8x + 8z + 9 \tag{3}$$

$$N_{TSV} = 16x + 21(z+1) \tag{4}$$

Considering Fig. 5 and at constant z, for a specific number of DC sources, the other parameters of PSMLI can be determined as:

$$N_{DC} = N_C = k \tag{5}$$

$$N_P = 4(k+1)$$
 (6)

$$N_V = 4k + 1 \tag{7}$$

$$N_{TSV} = 8k + 5 \tag{8}$$

Since power switches of the symmetrical cascaded z^{th} module have same TSV as the original module (n = 1), the TSV can be realized by:

$$TSV_{n=1} = TSV_{z1} = TSV_{z2} \tag{9}$$

Considering a constant number of cascaded modules, the voltage stress of the switches of the symmetrical submodules can be determined by:

$$V_{S_{(7x-6,7)}} = V_{S_{(7x-5,7)}} = V_{S_{(7x-2,7)}} = 2V_{DC}$$
(10)

$$V_{S_{(7x-3,z)}} = V_{S_{(7x-1,z)}} = 4V_{DC}$$
 (11)

$$V_{S_{(7x-4,z)}} = V_{S_{(7x,z)}} = V_{DC}$$
(12)

111313

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FIGURE 6. The characteristics of extended asymmetrical PSMLI module in terms of voltage level (N_V) .

C. MODULARITY OF ASYMMETRIC MODULE

Although asymmetrical MLI structures induces superfluous voltage stress and imbalance into the system, it is one of the simplest methods of boosting voltage levels without introducing any structural complexity or usage of higher number of power electric components. The proposed PSMLI can also be extended using asymmetrical module. In order to maximize the voltage level, the second submodule or of the PSMLI is designed with voltage sources with tertiary voltage capability (i.e., $V_{DC(1,0)} = V_{DC(2,0)} = 3E$) or in other words, a voltage ratio of 1:3 is maintained between the original module and the extended module. Thus, with the addition of only 8 switches the extended PSMLI would have the ability to generate 33 voltage levels. For synthesizing similar number of voltage levels, a symmetrical PSMLI would require 3 extra submodules (i.e., x = 3) or 36 power switches according to (2) and (6). However, the TSV of the entire PSMLI would increase to $69V_{DC}$. The relation between the voltage levels and voltage stress are shown in Fig. 6 for further comprehension. Similar to the symmetrical extension of PSMLI, the equations for the asymmetrical extension can be realized by:

$$N_V = 3(8x + 8z + 9) \tag{13}$$

$$N_{TSV} = 48x + 63z + 21 \tag{14}$$

Considering a constant number of cascaded modules, the voltage stress of the switches of the asymmetrical submodules can be determined by:

$$V_{S_{(7x-6,z)}} = V_{S_{(7x-5,z)}} = V_{S_{(7x-2,z)}} = 6V_{DC}$$
(15)

$$V_{S_{(7x-3,z)}} = V_{S_{(7x-1,z)}} = 12V_{DC}$$
(16)

$$V_{S_{(7x-4,z)}} = V_{S_{(7x,z)}} = 3V_{DC}$$
(17)

D. EFFICIENCY AND LOSS PROFILE OF PSMLI

The suggested MLI configuration's efficiency and power loss are assessed using the PLECS software. The power loss evaluation on all heat sinks is done in the steady-state condition maintaining an ambient temperature of 25°C. Heat is distributed evenly across the heat sinks. By using the data sheets, thermal profiles of diodes and IGBTs are computed automatically by PLECS software. The power loss of the PSMLI is predicted to be 900W under nominal working conditions. The efficiency is calculated by taking into account the conduction and switching losses of switching devices, as well as the power losses of switched capacitors. The capacitor generated losses are calculated as follows:

$$P_{cap} = P_D + P_R \tag{18}$$

$$P_D = (0.1\mu_{DC})^2 \times \pi \times f \times C \times \tan \delta_0 \qquad (19)$$

$$P_R = I^2 R_S \tag{20}$$

The resistive and dielectric losses are represented by P_R and P_D , respectively. Furthermore, the maximum DC voltage of a capacitor is denoted by μ_{DC} , f represents the fundamental frequency, which is 50 Hz, C symbolizes the capacitance, dissipation factor is depicted by tan δ_0 that is 0.15. Utilizing (18) – (20), the capacitor losses are 11.8 W. The diodes' switching and conduction losses at steady state are 0.012 W and 0.871 W, respectively, while the total IGBTs' switching, and conduction losses are 0.193 W and 9.187 W. The overall efficiency is 94.5%, with a total power loss of 22.063 W.

E. VOLTAGE RIPPLE CALCULATION OF PSMLI

For a high-quality AC output, a constant total DC-link voltage is necessary. In order to avoid a significant amount of voltage ripple, a switchable capacitor must have a voltage ripple of no more than 5%. The following calculation can be used to calculate the voltage ripples of both capacitors:

$$\Delta V_C = \frac{1}{\omega C} \int_{\theta_{on}}^{\theta_{off}} i_0 \, d\omega t \tag{21}$$

Using PSMLI's basic output current, this may be figured out further as follows:

$$\Delta V_C = \frac{I_{AB}}{\omega C} \int_{\theta_{on}}^{\theta_{off}} \sin(\omega t - \varphi) \, d\omega t \tag{22}$$

Here, φ indicates the angular shift between voltage and current, ω indicates the angular frequency of the multilevel AC voltage, ripple voltage end angle is indicated by θ_{off} , ripple voltage starting angle is indicated by θ_{on} , capacitance of capacitors is indicated by *C*. Using the following equations, the ripple angle can be calculated as:

$$\theta_{on} = \sin^{-1} \left[\frac{N_{VR} + 0.5}{Q \times m(N_C + 1)} \right]$$
(23)

$$\theta_{off} = \pi - \theta_{on} \tag{24}$$

where, the quality factor is indicated by Q and modulation index is indicated by m. The capacitor voltage ripple level is indicated by N_{VR} . Both capacitors' voltage ripples are computed, and the computed value is 3.23 V. This determines that low ripples exist in the capacitor voltage, and the proposed MLI can be implemented effectively.



FIGURE 7. Voltage level (N_V) vs TSV of extended PSMLI for configuration-1 and configuration-2.

III. OPTIMIZED PSMLI TOPOLOGY

By choosing an optimum structure for each module, the TSV of the extended symmetrical PSMLI can be reduced. Here, the asymmetric PSMLI is not considered because of drawbacks associated with those modules such as high TSV and voltage imbalance which can cause serious problems specially in renewable energy applications. A specific combination of x (submodules) and z (cascaded modules) must be chosen to develop the proposed PSMLI's extended structure having minimum voltage stress. This optimum configuration also ensures that a reduced number of power electric components are fully utilized. Thus, the voltage levels (N_V) and corresponding TSV for two alternative configurations of PSMLI under different values of x and z can be plotted to find the optimal configuration.

A. CONFIGURATION 1

The PSMLI can be designed with any number of cascaded or z^{th} modules, each having one cross connected submodule (x = 1). Under this configuration with the number of voltage levels that can be produced by the proposed inverter is found using (3) which is 8z + 17. On the other hand, the TSV of the whole inverter can be determined by utilizing (4).

B. CONFIGURATION 2

The PSMLI can be designed with only cascaded module (*z*) and several submodules (x > 1) in this configuration. Under these circumstances (configuration-1 and configuration-2), the number of voltage levels (N_V) and TSV of the novel MLI can be again determined using (3) and (4) respectively. The graphical representation of N_V vs TSV is illustrated Fig. 7. It is visible from Fig. 7 that in terms of TSV configuration-2 is more feasible than configuration-1. The higher THD of configuration-1 is due to the utilization of 4 extra switches while adding several cascaded modules. Thus, the overall cost of configuration-1 will be much higher than configuration-2 since switches with high voltage ratings are highly expensive [28]. However, in terms of simplicity and switching control, configuration-1 is preferable since it can be built with

TABLE 2.	Comparative	analysis	between	MLIs.
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MIT.	M	N	N	N	TOM	Boosting	H-
MLIS	N_{DC}	N_P	N _{Vmax}	N_V	187	Factor	bridge
NPC	1	4(<i>n</i> + 3)	<i>n</i> + 3	2 <i>n</i> + 7	4(n+3)	0	No
FC	1	4(<i>n</i> + 3)	<i>n</i> + 3	2n + 7	4(<i>n</i> + 3)	0	No
CHB	<i>n</i> + 3	4(<i>n</i> + 3)	<i>n</i> + 3	2n + 7	4(n+3)	0	Yes
[9]	2(<i>n</i> + 1)	2(3n + 5)	2(n + 1)	4n + 5	14(n+1)	0	Yes
[10]	<i>n</i> + 3	2(2n+5)	<i>n</i> + 3	2n + 7	4(4 <i>n</i> + 1)	0	Yes
[11]	<i>n</i> + 3	5 <i>n</i> + 14	<i>n</i> + 3	2n + 7	25 <i>n</i> + 6	0	Yes
[12]	<i>n</i> + 3	2(2n+3)	<i>n</i> + 3	2n + 7	16(<i>n</i> +1)	0	Yes
[13]	<i>n</i> + 3	4(<i>n</i> + 3)	2(n + 1)	4n + 5	8(2 <i>n</i> + 3)	0	Yes
[14]	<i>n</i> + 3	4(<i>n</i> + 2)	<i>n</i> + 3	2n + 7	2(11n + 1)	0	Yes
[15]	<i>n</i> + 3	2(<i>n</i> + 6)	<i>n</i> + 3	2n + 7	6(<i>n</i> + 6)	0	Yes
[16]	2(n+1)	5 <i>n</i> + 7	2(n+1)	4n + 5	13 <i>n</i> + 19	0	No
[17]	<i>n</i> + 3	3 <i>n</i> + 7	<i>n</i> + 3	2n + 7	12 <i>n</i> + 7	0	No
[18]	2n	5 <i>n</i> + 9	2(n+1)	4n + 5	10(n+1)	2	No
[19]	<i>n</i> + 4	2 <i>n</i> + 10	<i>n</i> + 4	2n + 9	2(4 <i>n</i> + 9)	0	No
[20]	<i>n</i> + 3	4(<i>n</i> + 2)	<i>n</i> + 3	2n + 7	10(<i>n</i> + 2)	0	No
[22]	1	12 <i>n</i>	3 <i>n</i>	6 <i>n</i> + 1	16 <i>n</i>	3	No
[23]	1	16 <i>n</i>	3 <i>n</i>	6n + 1	16 <i>n</i>	3	No
[24]	1	14 <i>n</i>	3 <i>n</i>	6n + 1	22 <i>n</i>	4	No
[25]	1	10 <i>n</i>	3 <i>n</i>	6n + 1	32 <i>n</i>	3	Yes
[26]	1	13 <i>n</i>	3 <i>n</i>	6n + 1	23 <i>n</i>	4	Yes
[27]	1	12 <i>n</i>	3 <i>n</i>	6n + 1	22 <i>n</i>	3	No
PSMLI	2 <i>n</i>	4(2n + 1)	4 <i>n</i>	8n + 1	8(<i>n</i> +1)	2	No

similar cascaded modules and same switching sequences. In terms of power switches, configuration-2 is more costeffective since it requires a smaller number of power switches for generating higher voltage levels. Configuration-2 can generate 81-level voltage utilizing 84 power switches while configuration-1 requires 112 power switches for generating same voltage level. Considering all these advantageous aspects, this manuscript gives more emphasis on configuration 2.

IV. COMPARATIVE ANALYSIS

In order to justify PSMLI's superiority in terms of usage of lesser number power electronic components, a comprehensive comparative analysis is presented in this section with classical and other recently proposed MLIs. For comparison, the symmetrical version is selected for each MLI.

Configuration-2 of PSMLI is selected for this analysis since it is more optimized than configuration-1. The parameters that are chosen to conduct this comparison: number of DC sources (N_{DC}), number of power switches (N_P), number of voltage levels (N_V), maximum voltage (N_{Vmax}), TSV, boosting factor and requirement of H-bridge circuit. The generalized equations of the MLIs are shown in Table 2.

In comparison with the classical MLIs it can be observed that the proposed MLI has used low number of power switches. The classical NPC inverters require a smaller number of DC sources compared to PSMLI. However, it requires huge number of switches [refer to Fig. 8(a)], clamping diodes and capacitors to generate greater voltage levels. Thus, it has serious voltage imbalance issues which requires the application of complex modulation techniques



FIGURE 8. Comparative analysis among different MLIs in terms of: (a) switches (N_P), (b) DC sources (N_{DC}), (c) TSV (N_{TSV}).

to be resolved. FC MLIs also requires small number of DC sources but has the characteristics of using large number of capacitors and power switches as shown in Fig. 8(a) which can greatly hamper the efficiency of the MLI by inducing capacitor losses in the system. CHB MLI requires large number of switches and DC sources compare to the proposed MLI as illustrated in Fig. 8(a) and 8(b) respectively. Symmetric CCMLI [15] requires 14 switches and 5 DC sources to generate 9-level output which is more than the proposed MLI. In addition, the TSV of the CCMLI is $42V_{DC}$ as shown in Fig. 8(c) which is substantially greater than PSMLI.

A similar attribute can be observed in the MLIs proposed in [16]–[20] where, large number of switches and DC sources are required compared to PSMLI. The proposed MLI in [17], [19] require same number of switches as PSMLI for the basic configuration (n = 1). However, as the voltage level increases, they require a greater number of DC sources and switches evidential from Fig. 7(c). On the other hand, the MLIs proposed in [16]–[20], [22]–[24], [27] avoided the use of H-bridge. However, they require high number of power switches.

The proposed MLI is also compared with similar class of switched capacitors MLIs (SCMLI) proposed in [22]–[27]. It can be observed from Fig. 8(b) that although these MLIs utilized a single DC source, they tend to have higher TSV [refer to Fig. 8(c)] and uses increased number of switching devices [refer to Fig. 8(a)] compared to the proposed MLI.

It is further noticeable that the boosting factor is only present for the MLIs that are comprised of switched capacitors units. This provides an added advantage to these MLIs since they do not require high number of isolated DC sources and transformers. The highest boosting factor is provided by the MLIs proposed in [24] and [26] as shown in Table 2. Both of these modules used single DC source to produce 9-level output at n = 1. On the contrary, the SCMLIs proposed in [22], [23], [25], and [27] have a triple boosting ability. Although, these MLIs have higher boosting ability than the proposed MLI, they have utilized high number of power switches and also induced high TSV which is evident from Fig. 8(a) and Fig. 8(c), respectively. Thus, it can

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be stated that the proposed PSMLI has created a balance among the utilization of power electronic components such as switch and DC sources, voltage boosting ability, and TSV.

PSMLI's superiority is further validated by comparing it with other MLIs in terms power losses and efficiencies. The power losses and efficiencies are obtained using PLECS software. The MLIs are built with similar model of power electronic switches, DC sources, diodes and capacitors to justify the comparison. Furthermore, a maximum DC-link voltage of 200 V is considered for the MLIs with an operating power of 900 W. The efficiencies (η) of each MLI are determined by considering three types of losses which are conduction losses (P_{con}) , switching losses (P_{sw}) and capacitor losses (P_{cap}) . The power loss data obtained from PLECS software is then added to determine the total power losses (P_{total}) of each MLI as demonstrated in Table 3. It can be observed from Table 3 that PSMLI's efficiency is less than the MLIs proposed in [16]-[20]. It is due to the fact that these MLIs does not incorporates any capacitors and hence, there is no capacitor loss. Nevertheless, all these MLIs use several DC sources which can massively increase their building costs. It should be addressed that the SCMLIs' efficiency is calculated for generating 7-level voltage. Yet, the proposed MLI has higher efficiency than all SCMLIs.

V. RESULTS AND DISCUSSIONS

The operation of the proposed PSMLI is validated in this section by presenting the simulation and experimental results. Similar parameter settings are selected for both simulation and experimental setup to justify and compare the results.

A. SIMULATION RESULTS

MATLAB Simulink is used to simulate the proposed PSMLI. The 9-levels (n = 1) output voltage of PSMLI is illustrated in Fig. 9(a) using the NLC modulation technique. Here, each voltage level is 10 V to create a 50 Hz multilevel staircase output voltage of 40 V. The harmonic spectrum of the 9-levels output voltage is depicted in Fig. 9(b). Furthermore, the 17-levels (n = 2) output voltage and

 TABLE 3. Power loss and efficiency comparison.

MLIs	$P_{con}\left(\mathrm{W}\right)$	$P_{sw}(\mathbf{W})$	$P_{cap}\left(\mathbf{W}\right)$	$P_{total}(W)$	η (%)
NPC	9.49	0.12	23.66	33.27	91.68
FC	8.43	0.14	73.12	81.69	79.58
CHB	8.67	0.14	0	8.81	97.83
[9]	18.45	0.22	0	18.67	95.33
[10]	22.40	0.15	0	22.55	94.36
[11]	38.80	0.28	0	39.08	90.23
[12]	21.08	0.07	0	21.15	94.71
[13]	42.16	0.30	0	42.46	89.39
[14]	18.97	0.09	0	19.06	95.24
[15]	19.37	0.28	0	19.65	95.09
[16]	12.65	0.18	0	12.83	96.79
[17]	6.26	0.15	0	6.41	98.40
[18]	9.22	0.13	11.83	21.18	94.70
[19]	5.93	0.08	0	6.01	98.49
[20]	11.86	0.17	0	12.03	96.98
[22]	6.32	0.09	11.80	18.21	95.45
[23]	8.43	0.12	11.79	20.34	94.92
[24]	10.14	0.14	11.81	22.09	94.48
[25]	10.54	0.30	11.80	22.64	94.34
[26]	9.85	0.14	29.48	39.47	90.13
PSMLI	9.20	0.21	11.80	22.06	95.54



FIGURE 9. Simulation results of basic PSMLI: (a) 9-levels output voltage, (b) harmonic spectrum.



FIGURE 10. Simulation results of extended PSMLI: (a) 17-levels output voltage, (b) harmonic spectrum.

harmonic spectrum of the cascaded PSMLI are shown in Fig. 10(a) and Fig. 10(b) respectively. Having the same individual voltage level of 10 V, this cascaded module is able to generate 80 V output. It can be noticed that in terms of THD, the extended configuration performed much better than the basic configuration since it produced almost double amount of voltage level. Therefore, the THD of this module has effectively fulfilled the IEEE 519 standard. The

TABLE 4. Power loss and efficiency comparison.

Components	Model	Specifications
IGBT switches	IGB30H60H3	600 V, 30 A
Gate drivers IC	SN7411C04N	10-35 V, 1.5 A
Diodes	MUR1560G	600 V, 15 A
Capacitors	ESM1201VSN272MA50S	200 V, 2700 µF
Frequency	-	50 Hz
Load value	R-L	$40 \Omega - 5 \text{ mH}$
Load variation	R	100 Ω – 160 Ω
Non-linear load	KBPC2510	1-phase, 25 A, 1kV
DC-link voltages	CSI3003X3	20 V
Harmonics Analyzer	Fluke 43B	-
DSP	TMS320F28335	150 MHz
Components	Model	Specifications



FIGURE 11. Hardware prototype of PSMLI.



FIGURE 12. Experimental results of the basic 9-level PSMLI.

THD of 9-level PSMLI can be improved by implementing selective harmonic elimination (SHE) control where the switching angle of each power switch is individually optimized [28].

B. EXPERIMENTAL RESULTS

The parameters and the model of the components used to build the hardware model is shown in Table 4. The hardware setup is shown in Fig. 11 which include all the power components.

The experimental results of the 9-level (n = 1) and 17-level (n = 2) symmetrical PSMLI's voltage waveforms are presented in Fig. 12 and Fig. 13, subsequently along with



FIGURE 13. Experimental results of the basic 17-level PSMLI.



FIGURE 14. THD results obtained from Fluke 43B for: (a) 9-level PSMLI, (b) 17-level PSMLI.

the harmonic spectrums in Fig. 14(a) and Fig. 14(b). The results are obtained with a fundamental frequency of f = 50, modulation index m = 1, and inductive load of $(40 \Omega - 5 \text{ mH})$. It can be noticed that the basic configuration of PSMLI has synthesized 9-level voltage with a peak magnitude of 43.04 V. In contrast, the extended PSMLI has produced 17-level voltage with a magnitude of 81.16 V. In terms of THD the extended module performed better than the basic module since it produced higher voltage level. Thus, the THD of 17-level module has met the IEEE 519 2014 voltage harmonics standard (i.e., THD < 8%). Moreover, the voltage and current waveform of the asymmetrical 33-level PSMLI is shown in Fig. 15. It is clearly observable that the voltage waveform has become nearly identical to a pure sine wave. Thus, the THD in this case has further decreased to only 2.58% while the voltage has increased to 162.59 V. Finally, it can be seen from Fig. 16 that the capacitor voltages for both capacitors are balanced and stable while the prototype of the PSMLI module is operating at nominal condition. It further indicates that the hardware model of the proposed PSMLI is performing without any major issue.

The performance of the PSMLI is tested in 3 different transient conditions and results are shown in Fig. 17. In 1st case, the input DC voltage is altered from 10 V to 5 V. As a result, it is noticeable from Fig. 17(a) that the output voltage is decreased from 43.04 V to 20.22 V while the current decreased from 1.34 A to 0.65 A. Nevertheless, the MLI is



FIGURE 15. Experimental results of the asymmetrical 33-level PSMLI.



FIGURE 16. Balanced capacitor voltages of the PSMLI.

working without any issue. In 2nd case, the modulation index is varied from $m = 1 \rightarrow 0.5 \rightarrow 0.3$ and thus, the voltage is decreased from 9-level \rightarrow 5-level \rightarrow 3-level as shown in Fig. 17(b). Although, the MLI is performing properly the THD of the output voltage increased from 9.7% \rightarrow 18.2% \rightarrow 29.1% since the MLI's voltage level is reduced. In the 3rd and final case, the load is varied gradually from 100 Ω to 160 Ω . Thus, the current is gradually decreased as illustrated in Fig. 17(c).

The capacitor voltages of the PSMLI are also observed under the transient conditions mentioned above. It can be observed from Fig. 18(a) that during the voltage fluctuations the capacitor voltages are also reduced to 5 V as the total voltage become 20.22 V. Nevertheless, it can be seen that the proposed PSMLI is functioning without any issues and the capacitor voltages are balanced even after the voltage fluctuation has occurred. During the change in modulation index and load from Fig. 18(b) and Fig. 18(c) respectively, it is noticeable that there is no change in the capacitor voltages. Therefore, it can be stated that the change in modulation index or the load does not have any impact on the capacitors' performance.

Finally, the performance of PSMLI is investigated under non-linear load conditions where the output of the MLI is connected with a single-phase bridge rectifier and inductive load (40 Ω – 5 mH). The 9-level output voltage can be observed to be completely similar to the previous case studies as shown in Fig. 19. However, the current of the PSMLI has slight distortions which is due to the fact the non-linear load



FIGURE 17. Performance evaluation of the PSMLI under different transient conditions: (a) voltage fluctuations, (b) variation in modulation index, (c) load transient.



FIGURE 18. Performance evaluation of the capacitor voltages of PSMLI under different transient conditions: (a) voltage fluctuations, (b) variation in modulation index, (c) load transient.



FIGURE 19. Experimental results of the basic 9-level PSMLI with non-linear load.

has induced current harmonics into the system. This issue can be effectively dealt with custom power devices such as shunt active power filters [3], [4].

VI. CONCLUSION

This manuscript presents a novel multilevel inverter unit that employs 2 DC sources and 2 switched capacitors to produce 9 voltage levels. The PSMLI is built utilizing a T-type inverter and a directional module that are put together back-to-back and encircled by extra switches. It can be extended effectively or can be designed using both symmetric and asymmetric DC-links to achieve higher output voltage. Additionally, it has comparatively reduced TSV and power electric components since it is a self-balanced MLI i.e., it does not require any additional power components to balance the capacitor voltages. PSMLI's another advantage is its ability to generate negative voltage without the need of an additional H-bridge unit. This has also contributed to its lower TSV and structural simplicity. The PSMLI unit is simulated and experimentally assessed, and it shows good results on both occasions. There is a high similarity between the simulated and experimental results which validates its accurate operation. A high efficiency of 95.54% is obtained which is better than most of the recently proposed MLIs as demonstrated in the comparative analysis section. PSMLI also achieved a low THD of 6.4% and 2.58% for 17level module and 33-level module, respectively and have successfully followed IEEE 519 2014 standard. The results also showed that the capacitor voltages of PSMLI are balanced with a very low voltage ripple of 3.23 V. These results indicate the industrial suitability of the proposed module.

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SHEIKH T. MERAJ received the B.Sc. degree in electrical and electronic engineering from the Ahsanullah University of Science and Technology, Dhaka, Bangladesh, in 2015, and the M.Eng. degree from the Department of Electrical and Computer Engineering, Curtin University, Miri, Malaysia, in 2018. He is currently working as a Graduate Assistant (GA) with the Department of Electrical and Electronic Engineering, Universiti Teknologi PETRONAS (UTP), Perak, Malaysia,

where he is concurrently working as an Assistant Lecturer. He is actively involved in research-based work with specific research focuses on power electronics, power quality, renewable energy integration, energy management schemes, and hydrogen energy and applications. He is also an active reviewer in multiple IEEE TRANSACTIONS.



M. S. ABD RAHMAN received the B.Eng. (Hons.) and Ph.D. degrees in electrical engineering from the University of Southampton, U.K., in 2010 and 2014, respectively. Currently, he is a Senior Lecturer with the Department of Electrical Power Engineering, Universiti Tenaga Nasional. His research interests include the high voltage condition monitoring, power systems, and power electronics.



NOR ZAIHAR YAHAYA (Senior Member, IEEE) was born in Lumut, Malaysia. He received the B.Sc. degree in electrical engineering from the University of Missouri-Kansas City, USA, in 1996, the M.Sc. degree in microelectronics from the University of Newcastle Upon Tyne, U.K., in 2002, and the Ph.D. degree from Universiti Teknologi PETRONAS, Malaysia, in 2011. He is currently an associate professor, teaching and doing research in the area of power electronics

and drives. He has published more than 70 papers in proceedings, journals, and book chapter with several patent and copyright granted. He is also actively working on projects related to renewable energy applications for the government, industry, and PETRONAS.



PIN JERN KER (Senior Member, IEEE) received the B.Eng. degree (Hons.) in electrical and electronic engineering from Universiti Tenaga Nasional (UNITEN), Malaysia, in 2009, and the Ph.D. degree in electronic and electrical engineering from The University of Sheffield, U.K. Currently, he is a Senior Lecturer with the Department of Electrical Power Engineering, UNITEN, where he is also the Head of the Electronics and IT Unit, Institute of Power Engineering. His research

interests include the simulation and characterization of photodetectors, optical sensing, design of monitoring, and control systems for energy-related applications.



KASHEM M. MUTTAQI (Senior Member, IEEE) received the B.Sc. degree in electrical and electronic engineering from the Bangladesh University of Engineering and Technology (BUET), Dhaka, Bangladesh, in 1993, the M.Sc. degree in electrical engineering from the University of Malaya, Kuala Lumpur, Malaysia, in 1996, and the Ph.D. degree in electrical engineering from Multimedia University, Selangor, Malaysia, in 2001. He is currently a Professor with the School of Electrical, Computer,

and Telecommunications Engineering; and a member of the Australian Power Quality and Reliability Center (APQRC), University of Wollongong, Wollongong, Australia. His research interests include distributed generation, renewable energy, electrical vehicles, smart-grid, power systems planning, and emergency control.



TOUHID M. HOSSAIN received the B.Sc. degree in computer engineering from Independent University Bangladesh (IUB), Bangladesh, in 2016, and the M.Sc. degree in information technology from Universiti Teknologi PETRONAS (UTP), Malaysia, in 2021. Currently, he is working as a Research Scientist with UTP. His research interests include soft computing, explainable machine learning, data science, and knowledge computing.



M. S. HOSSAIN LIPU received the B.Sc. degree in electrical and electronic engineering from the Islamic University of Technology, Bangladesh, in 2008, the M.Sc. degree in energy from the Asian Institute of Technology, Thailand, in 2013, and the Ph.D. degree from the Department of Electrical, Electronic and Systems Engineering, National University of Malaysia, in 2019. Currently, he is an Associate Professor with the Department of Electrical and Electronic Engineering, Green University of Bangladesh (GUB). Prior to joining GUB, he worked as a

Senior Lecturer with the Department of Electrical, Electronic, and Systems Engineering, National University of Malaysia; and an Assistant Professor with the Department of Electrical and Electronic Engineering, University of Asia Pacific, Bangladesh. His research interests include battery storage and management systems, electrical vehicles, power electronics, intelligent controllers, artificial intelligence, and optimization in renewable systems.



M. A. HANNAN (Senior Member, IEEE) received the B.Sc. degree in electrical and electronic engineering from the Chittagong University of Engineering and Technology, Chattogram, Bangladesh, in 1990, and the M.Sc. and Ph.D. degrees in electrical, electronic, and systems engineering from Universiti Kebangsaan Malaysia (UKM), Bangi, Malaysia, in 2003 and 2007, respectively. He was with the Bangladesh Power Development Board, from 1994 to 2001. He was with the

National University of Malavsia, where he became a Senior Lecturer, in 2008; an Associate Professor, in 2010; and a Full Professor, in 2013. He has been a Professor of intelligent systems with the Department of Electrical Power Engineering, College of Engineering, Universiti Tenaga Nasional, Malaysia, since September 2016. He has more than 28 years of industrial and academic experience and an author or a coauthor of over 300 papers published in international journals and conference proceedings. His research interests include intelligent controllers, power electronics, hybrid vehicles, energy storage systems, image and signal processing, and artificial intelligence. He is an Editorial Board Member of many journals. He has been received several IEEE best paper awards. He received numbers of gold awards for his innovative research in ITEX, MTE, INNOFEST, SIIF, and PERINTIS. He is the Organizing Chair of many conferences e.g., ICEE 2019 and PEAE 2019. He is the Editor-in-Chief of the journal Energy and Environment and an Associate Editor of IEEE Access and IEEE TRANSACTIONS ON INDUSTRY APPLICATIONS.

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